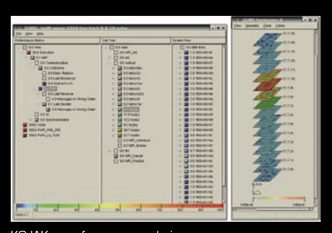
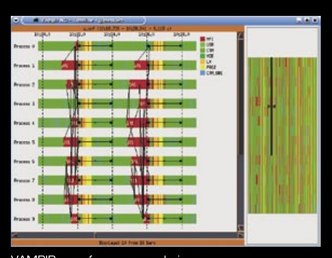
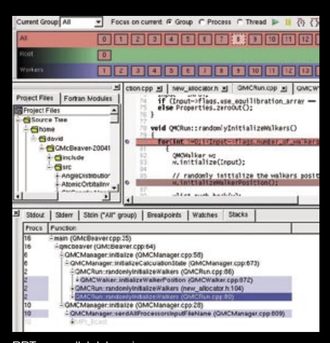
The *//ParMA* Project

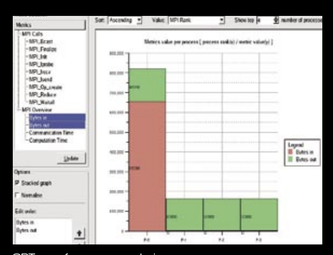
Parallel Programming for Multi-core Architectures

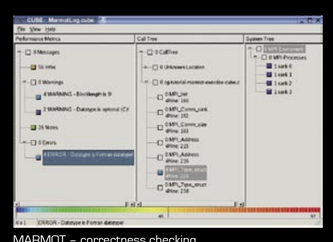
Develop advanced technologies to exploit fully the power of multi-core architectures
Improve the performance of conventional HPC applications
Enable the advent of power-intensive innovative embedded applications


KOJAK – performance analysis


VAMPIR – performance analysis


DDT – parallel debugging


OPT– performance analysis


MARMOT – correctness checking

Evolve methods and tools to facilitate the development (or restructuring) of parallel applications:

- Define new programming and execution models for parallel applications
- Define high-level directives for multilevel parallel programming
- Develop tools to create and model efficient interconnection networks for MPSoC, which will be the basis for embedded systems.

Enhance and integrate parallel programming tools (debuggers, correctness and performance analysis tools):

- Support different flavors of parallel/multithreaded applications (MPI, Open MP, POSIX Threads, Hybrid)
- Capture runtime information on different levels
- Offer a powerful, user-friendly and scalable environment to software engineers to support all levels of correctness and performance debugging in a common framework

Extend the Linux OS (NUMA API, Scheduler, etc.) and optimize libraries:

- Extend and enhance the management of a large number of parallel tasks / threads (e.g. optimize data exchange using the cache memory, adapt timer interrupts, exploit the Performance Monitoring Unit, etc.).
- Optimize numerical libraries by developing multithreaded versions thereof
- Provide the project partners with HPC and Embedded platforms for experimentation

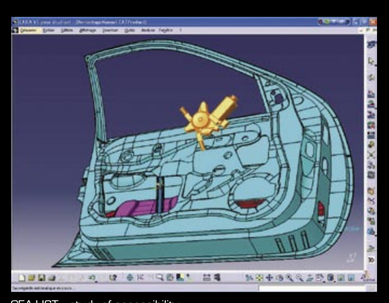
Use of advanced technology

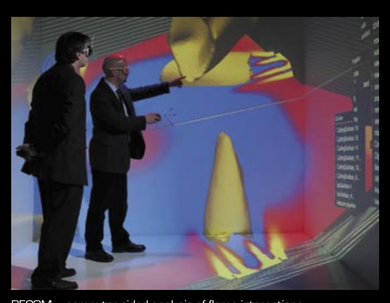
"The recent switch to parallel microprocessors is a milestone in the history of computing. [...] We believe that much can be learned by examining the success of parallelism at the extremes of the computing spectrum, namely embedded computing and high performance computing. [...] Since real world applications are naturally parallel and hardware is naturally parallel, what we need is a programming model, system software, and a supporting architecture that are naturally parallel. Researchers have the rare opportunity to re-invent these cornerstones of computing, provided they simplify the efficient programming of highly parallel systems."

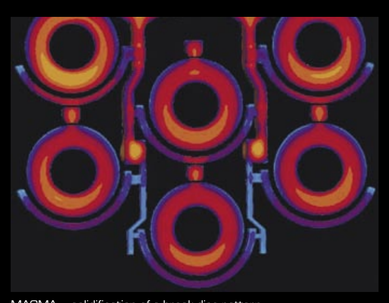
Feedback to technology providers

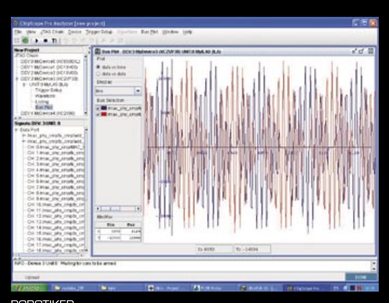
Adapt or develop and optimize applications from various application domains (Simulations, Avionics, Virtual Reality, Software Defined Radio):

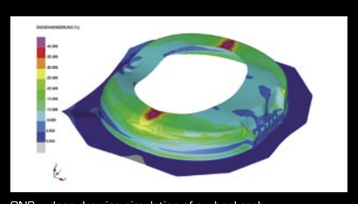
- Significantly speed-up existing applications and enable simulation of much more complex models and even process chains. For instance, due to virtual process design, product engineering costs in the automotive industry could be considerably reduced in the last years while, at the same time, requirements concerning crash safety, quality standards, weight reduction and time-to-market response were increasing.
- Enable the advent of innovative power-intensive embedded applications. For instance, in avionics, the intensive computational power needed to dynamically adapt the wing configuration with regard to speed, drag, and angle of incidence could not be envisaged so far because of the volume of the system, the power consumption, and the heat dissipation.


CEA-LIST – study of accessibility:
assembly of a control device of car door windows

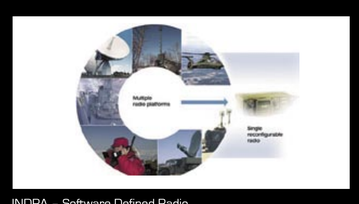

RECOM – computer-aided analysis of flame interactions
in a 300 MWe combustion chamber in the Virtual Reality


MAGMA – solidification of a break disc pattern


ROBOTIKER –
IQ signals directly captured from FPGA by logic analyzer


GNS – deep drawing simulation of a wheel arch


Dassault Aviation – latest civil F7X aircraft



INDRA – Software Defined Radio

Author:

Krammer Bettina

phone: (+49 - 711) 685-65890
fax: (+49 - 711) 685-65832
e-mail: krammer@hlrs.de

HLRS – High Performance Computing Center Stuttgart

Nobelstr. 19, 70569 Stuttgart, Germany

Project Details:

Project name: ParMA
Project number: ITEA 2 - 06015
Project start: 1 st June 2007
Project end: 31 st May 2010
http://www.parma-itea2.org

Countries involved:

France
Germany
Spain
United Kingdom

Partners:

Allinea Software Ltd, UK
Bull S.A.S, F
CAPS-Entreprise, F
CEA – Commissariat à l'énergie atomique, F
DA – Dassault Aviation, F
FZJ – Forschungszentrum Jülich, D
GNS mbH – Gesellschaft für Numerische Simulation, D
GWT-TUD GmbH – Gesellschaft für Wissens- und Technologietransfer der TU Dresden mbH, D
HLRS – Universität Stuttgart, D
INDRA SISTEMAS S.A, E
INT – Institut National des Télécommunications, F
MAGMA Gießereitechnologie GmbH, D
RECOM Services GmbH, D
Fundación ROBOTIKER, E
UAB – Universitat Autònoma de Barcelona, E
UVSQ – Université de Versailles Saint Quentin, F
ZIH – Technische Universität Dresden, D

References:

Krste Asanovic, Ras Bodik, Bryan Christopher Catanzaro, Joseph James Gebis, Parry Husbands, Kurt Keutzer, David A. Patterson, William Lester Plishker, John Shalf, Samuel Webb Williams and Katherine A. Yelick. The Landscape of Parallel Computing Research: A View from Berkeley. Whitepaper, 18. Dez. 2006. http://www.eecs.berkeley.edu/Pubs/TechRpts/2006/EECS-2006-183.html